VECTRON INTERNATIONAL
A DOVER TECHNOLOGIES COMPANY

Product Data Sheet

FX-101

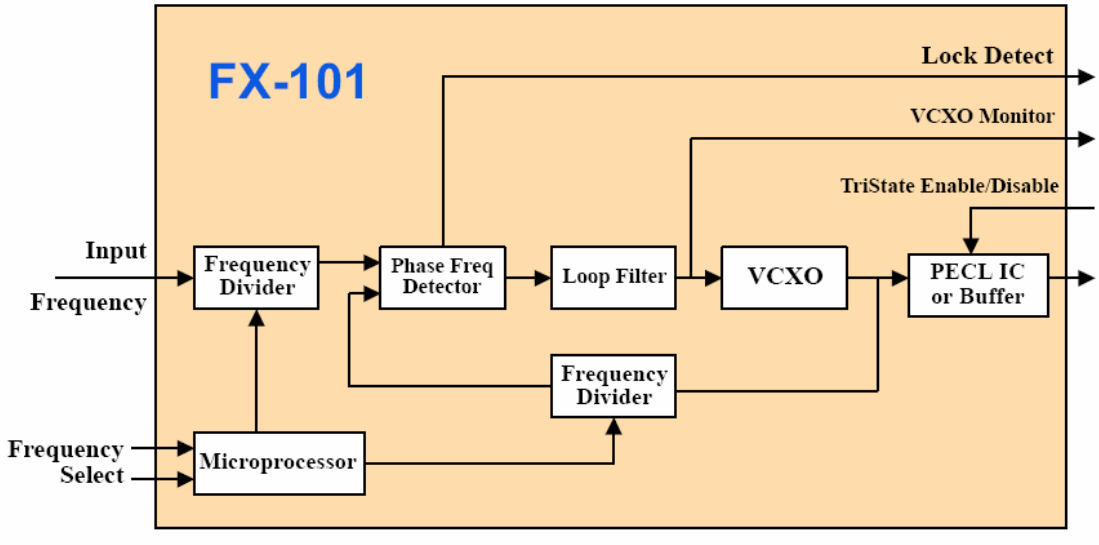
Frequency Translator

Features

- Output frequencies up to 77.760 MHz
- Locked to specified Input frequency, e.g. 8 kHz
- 1" x 0.8" x 0.2", Surface Mount (FR4 base)
- Single 5.0 Vdc or 3.3 Vdc supply
- Optional CMOS or PECL Output
- Low Output Jitter
- **RoHS/Lead Free Compliant**

Applications

- SONET / SDH / ATM / DSL-PON interconnects
- 8 kHz/16.384 MHz/19.44 MHz to 77.76 MHz
- 8 kHz/1.544 MHz/2.048 MHz to 44.736MHz



FX-101 Frequency Translator

Description

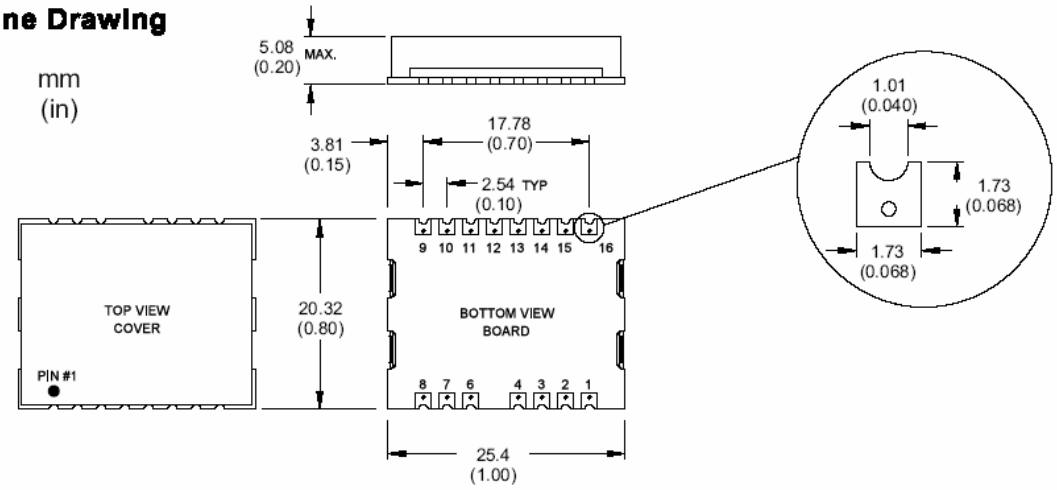
Vectron's FX-101 is a crystal based frequency translator which is used to translate any input frequency such as 8 kHz, 1.544 MHz, 2.048 MHz, 19.440 MHz etc. to any specific frequency less than or equal to 77.76 MHz. The input frequency does not have to be a 50/50% duty cycle and as an example can be an 8 kHz signal with a logic high "on time" of only 1us, such as a BITS clock. The FX-101 also has the ability to translate up to any of 4 different input frequencies to one common output frequency, such as input frequencies of 8 kHz and 1.544 MHz and 19.44 MHz and any other frequency between 333 Hz and 77.76 MHz translating them to an output frequency up to 77.76 MHz.

The "Input Frequency tracking capability" is the total amount of input frequency deviation in which the FX-101 is guaranteed to track or translate. As an example, a typical input clock would be 8 kHz ± 20 ppm. The FX-101 is guaranteed to track at least ±50 ppm of error over temperature/ aging/ power supply and is more than twice what most applications require. The PLL control voltage is brought out through a 470K ohm resistor. This would allow for the use of external circuitry (analog comparators or an A/D converter plus a processor) to detect when the control voltage is getting close to the limits of the pull range.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage, **C** = 5 Vdc **D** = 3.3 Vdc	V_{DD} V_{DD}	4.75 3.15	5.00 3.30	5.25 3.45	Vdc Vdc
Supply Current	I_{DD}		45	70	mA
Input Signal, "0" **A** = HCMOS	CLKIN	0		0.2(V_{DD})	Vdc
Input Signal, "1" **A** = HCMOS	CLKIN	0.7(V_{DD})		5.5	Vdc
OUTPUT, **F** = Comp PECL	---	---	PECL	---	---
V_{OH}	V_{OH}	V_{DD}-1.025		V_{DD}-0.880	Vdc
V_{OL}	V_{OL}	V_{DD}-1.810		V_{DD}-1.620	Vdc
Rise / Fall Time (77.76 MHz)	t_R/t_F		0.5	2	ns
OUTPUT, **A** = HCMOS	---	---	HCMOS	---	---
V_{OH}, I_{OL} = 50 uA	V_{OH}	V_{DD}-0.3			Vdc
V_{OL}, I_{OL} = 50 uA	V_{OL}			0.1	Vdc
Rise / Fall Time (77.76 MHz/20% to 80%)	t_R/t_F		1.4	2.5	ns
Output Symmetry, Freq >62.208 MHz and 3.3V	Sym Sym	45 40		55 60	% %
Jitter @ 77.76 MHz (rms 12 kHz to 20 MHz)			0.5	1.0	ps
Input Frequency Tracking Capability (Can translate a Stratum 1,2,3,3E,4 or SONET Min source)	APR	+/-50			ppm
Operating Temperature	Temp Range **C** = 0°C to +70°C Temp Range **F** = -40°C to +85°C				
Size	See page 3 for outline Drawings and Dimensions				

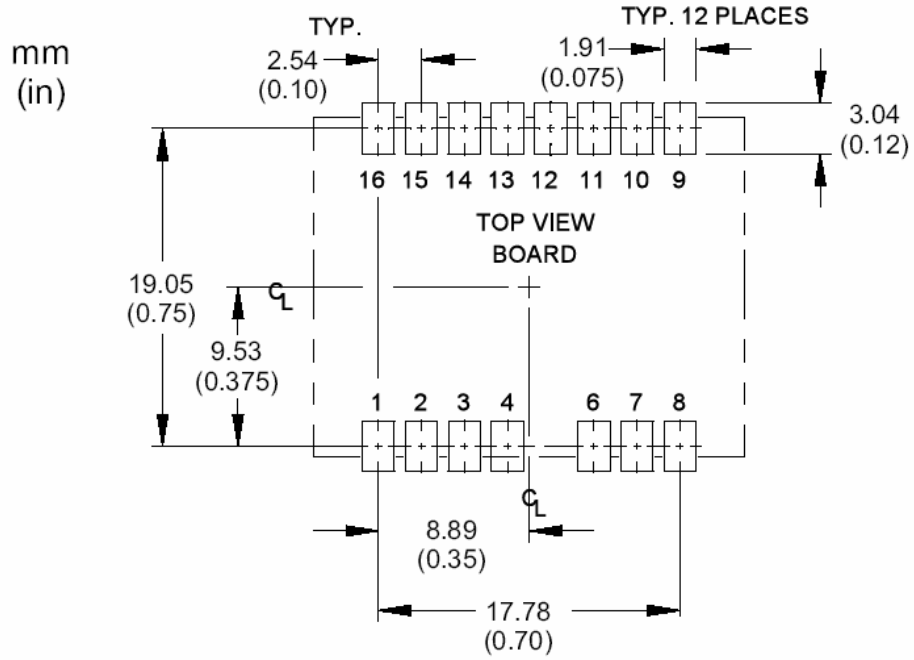
FX-101 Frequency Translator

Outline Drawing



Pin	Symbol	Function
1	CLKIN	Input Frequency
2	GND	Ground
3	LD (Output)	Lock Detect Logic "1" indicates a locked condition and requires a couple hundred pF capacitor to ground to operate correctly. Logic "0" indicates that no input signal is detected and can be used as a loss-of-signal alarm. Toggles when not locked.
4	Monitor (Output)	PLL/ VCXO control voltage Under locked conditions, should be >0.3V and <3.0 V for the 3.3 volt option or >0.5V and <4.5V for the 5 volt option. Input frequency may be out of range if voltage exceeds these limits.
5	NC	No Connection
6	NC	No Connection
7	GND	Ground
8	Tri-state (Input) Disable (Input)	TriState (**HCMOS output option**) Logic "1" (or no connect) = Output enabled Logic "0" = Output in high impedance Disable (**PECL output option**) Logic "1" = Output disabled Logic "0" (or no connect) = Output enabled
9	OUT	VCXO Output (PECL) or HCMOS Output
10	COUT	Complementary VCXO Output (PECL) or NC for HCMOS output option
11	NC	No Connection
12	Select A	Do not Exceed Vdd (NC for one input frequency)
13	Select B	Do not Exceed Vdd (NC for one or two input frequencies)
14	NC	No Connection
15	GND	Ground
16	V_{DD}	Power Supply Voltage (5 Vdc or 3.3 Vdc)

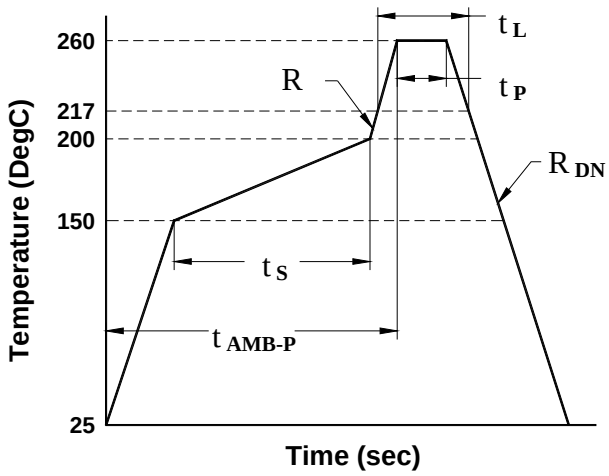
Recommended Land Pattern



Reflow Profile (IPC/JEDEC J-STD-020C)

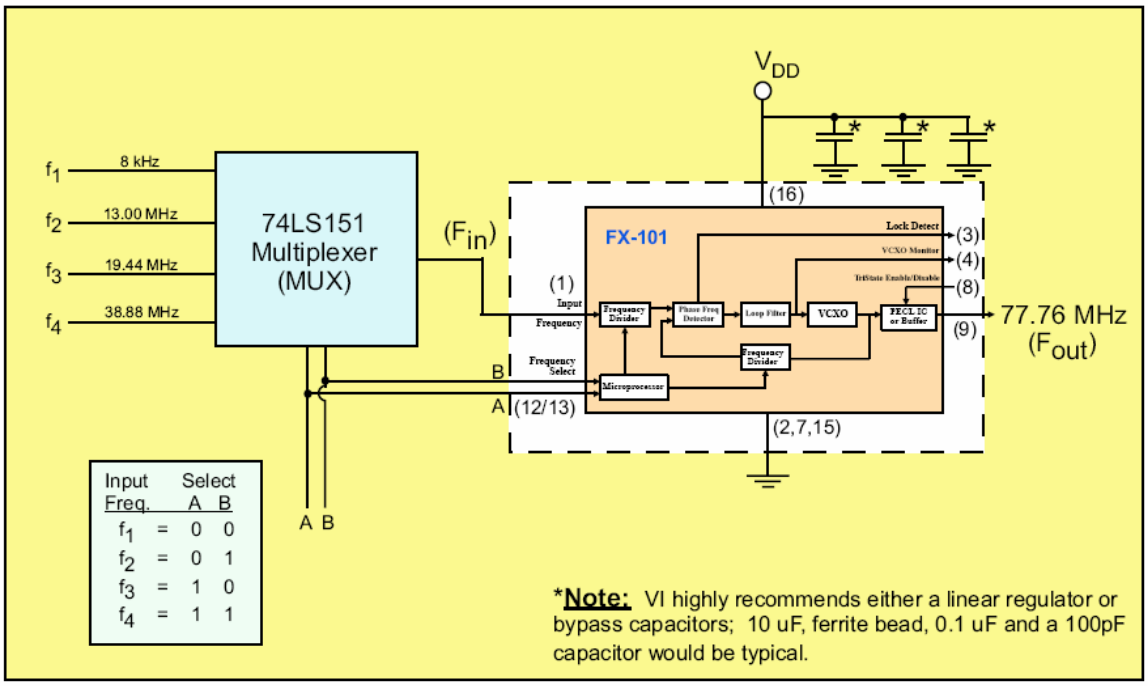
Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The FX-101 is being qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-101 should not be subjected to a wash process that will immerse it in solvents. NO CLEAN is the recommended procedure. The FX-101 has been designed for pick and place reflow soldering. The FX-101 may be reflowed once and should not be reflowed in the inverted position.



FX-101 Frequency Translator

Typical Application



All components outside the dotted line box are user supplied components and/or connections. This is just one possible configuration of the FX-101. For additional information about your specific needs please contact our Factory.

FAQ's

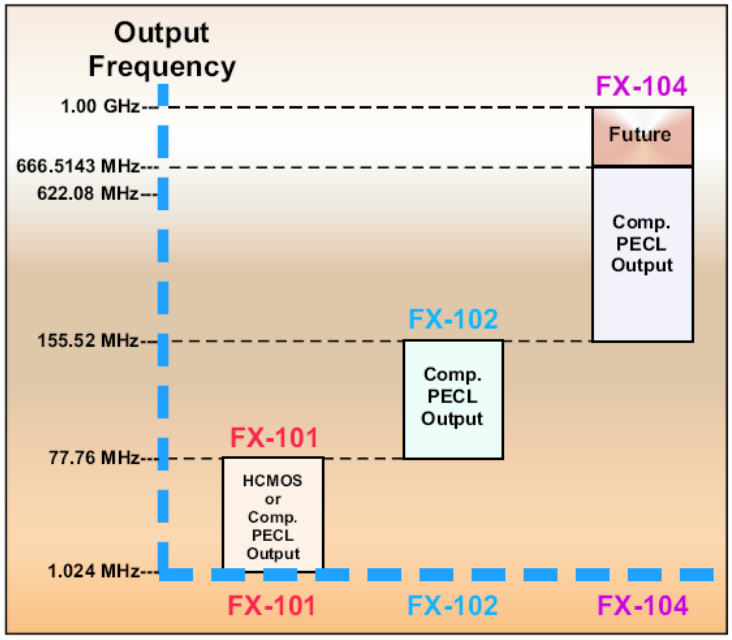
Q: What are the different input frequencies Available?
A: The FX-101 is able to handle any input frequency between 333 Hz and 77.76 MHz. (A list of standard frequencies is available on page 7.)

Q: How many different input frequencies can a specific FX-101 accept?
A: Each FX-101 can be programmed to accept up to 4 different frequencies.

Q: Does the output frequency need to be 77.76 MHz?
A: No, the output frequency can be any frequency between 1.024 MHz and 77.76 MHz. (A list of standard frequencies is available on page 7.)

Q: If there is only one input pin, how can your unit accept 4 different frequencies?
A: The customer is required to supply a multiplexer which would switch between the different input frequencies. The multiplexers' select pins would need to be sync'd to the select pins of the FX-101. (The drawing above illustrates this configuration.)

FX-100 Series Selection Guide



Handling Precautions

Although ESD protection circuitry has been designed into the FX-101 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation

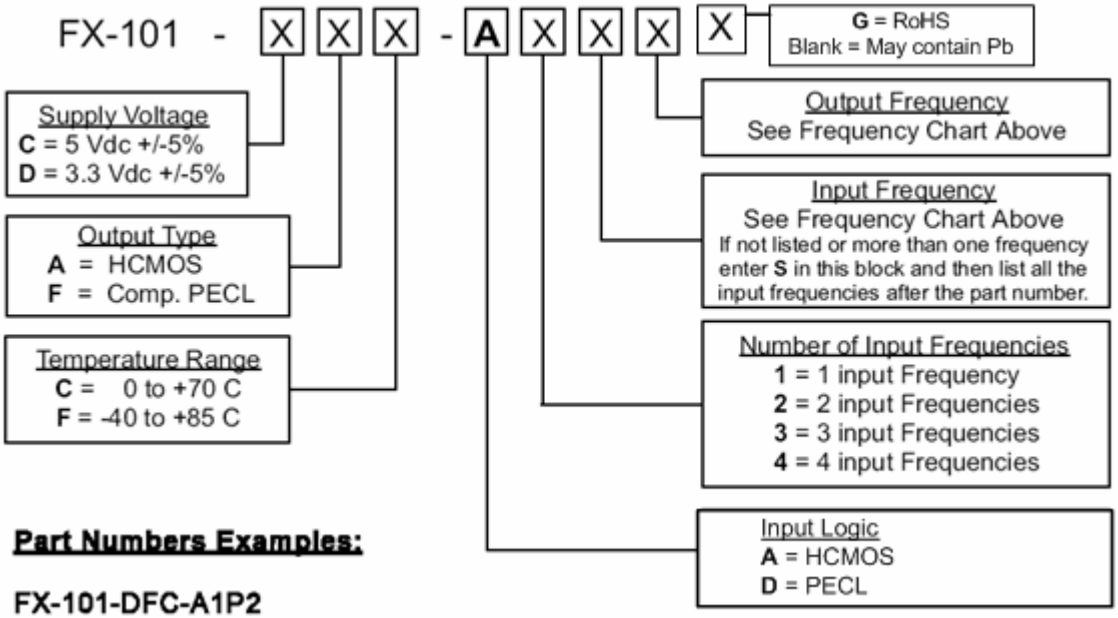
ESD Ratings

Model	Minimum	Conditions
Human Body Model	500 V	MIL-STD 883, Method 3015
Charged Device Model	500 V	JEDEC, JESD22-C101

FX-101 Frequency Translator

Standard Frequencies					
333 Hz	A	2.048 MHz	J	26.00 MHz	T
2 kHz	B	4.096 MHz	K	27.00 MHz	W
8 kHz	C	8.192 MHz	L	38.88 MHz	X
16 kHz	D	13.00 MHz	M	44.736 MHz	Y
64 kHz	E	16.384 MHz	N	51.84 MHz	0
1.024 MHz	F	19.44 MHz	P	61.44 MHz	1
1.544 MHz	H	20.48 MHz	R	77.76 MHz	2
		Special SCD	S		

How to Order



Part Numbers Examples:

FX-101-DFC-A1P2

FX-101-DAC-D1S2G – 8 kHz, 1.544 MHz, 2.048 MHz, 19.44 MHz

For Additional Information, Please Contact:

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