FX-427
Low Jitter Frequency Translator

Features

- **Quartz-based PLL for Ultra-Low Jitter**
- **Frequency Translation up to 850 MHz**
- **Accepts 4 externally-muxed clock inputs**
- **LVCMOS/LVDS/LVPECL Inputs Compatible**
- **Differential LVPECL Outputs**
- **Lock Detect**
- **Output Disable**
- **20.3 x 13.7 x 5.1 mm surface mount package**
- **Compliant to EC RoHS Directive**

Description

The FX-427 is a precision quartz-based frequency translator used to translate 1 to 4 selected input clocks as low as 8 kHz to an integer multiple as high as 850 MHz. The FX-427's superior jitter performance is achieved through the filtering action of the on-board voltage-controlled SAW oscillator (VCSO) and integrated loop filter. Two low-jitter outputs are provided. Monitoring and control functionality are also standard features.

Applications

- **Synchronous Ethernet**
- **Wireless Infrastructure**
- **802.16 BTS**
- **10 Gigabit FC**
- **10GbE LAN / WAN**
- **OADM and IP Routers**
- **Test Equipment**

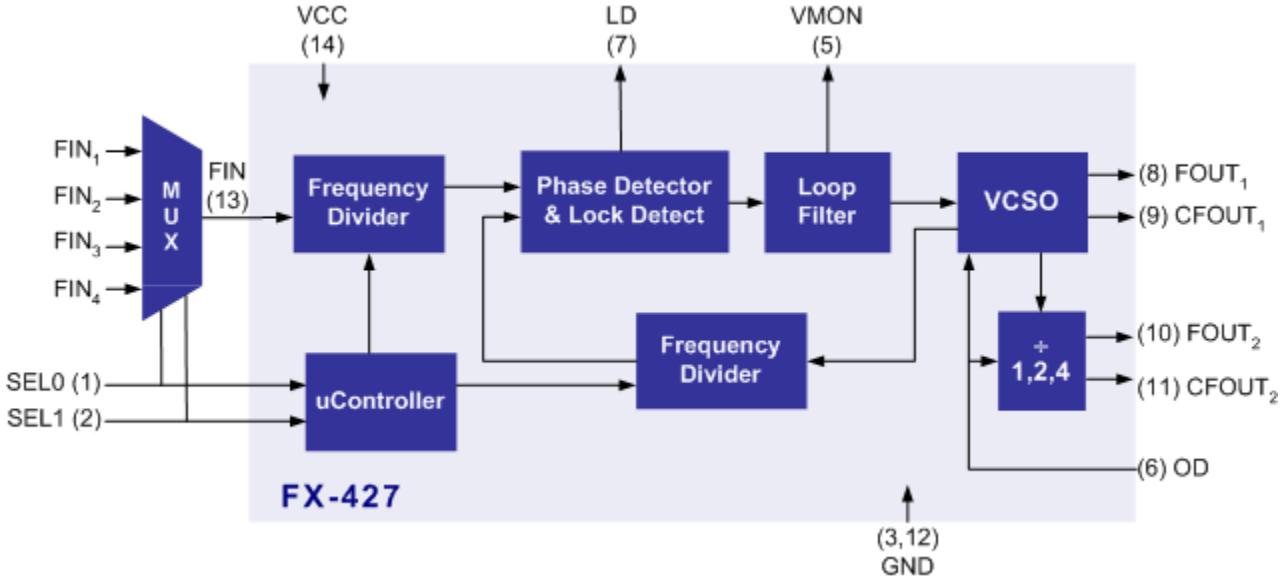


Figure 1. Functional Block Diagram

Table 1. Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency						
Input Frequency	F_{IN}	0.008		400	MHz	1,2,3
Capture Range	APR	±40			ppm	1,2,3
Output Frequency - Primary	F_{OUT1}	500		850	MHz	1,2,3
Output Frequency - Secondary	F_{OUT2}	125		850	MHz	1,2,3
Supply						
Voltage	V_{CC}	3.13	3.3	3.46	V	2,3
Current (No Load)	I_{CC}		140	180	mA	3
Input Signal						
LVCMOS	F_{IN}		LVCMOS			
LVDS	F_{IN}		LVDS			2,3,7
LVPECL	F_{IN}		LVPECL			
Differential Output (Options F and P)						
Common Mode Output Voltage	V_{OCM}	V_{CC}-1.5	V_{CC}-1.3	V_{CC}-1.1	V	3,5
DC Output High Voltage	V_{OH}	V_{CC}-1.085	V_{CC}-0.950	V_{CC}-0.880	V	3,5
DC Output Low Voltage	V_{OL}	V_{CC}-1.830	V_{CC}-1.700	V_{CC}-1.620	V	3,5
Peak-to-Peak Output Voltage	V_{P-P}		700		mV-pp	3,5
Rise Time	t_R		0.5		ns	4,5
Fall Time	t_F		0.5		ns	4,5
Symmetry	SYM	45	50	55	%	2,3
SSB Phase Noise, F_{OUT} **=** 155.52/622.08						
@ 10 Hz Offset	Φ_n		-64/-27		dBc/Hz	5,6
@ 100 Hz Offset	Φ_n		-95/-55		dBc/Hz	
@ 1 kHz Offset	Φ_n		-123/-85		dBc/Hz	
@ 10 kHz Offset	Φ_n		-143/-110		dBc/Hz	
@ 100 kHz Offset	Φ_n		-146/-130		dBc/Hz	
@ 1 MHz Offset	Φ_n		-146/-146		dBc/Hz	
@ 10 MHz Offset	Φ_n		-146/-146		dBc/Hz	
Jitter Generation						
155.52 MHz (12 kHz – 20 MHz BW)	Φ_J		0.30		ps RMS	5, 6
622.08 MHz (12 kHz – 20 MHz BW)	Φ_J		0.12		ps RMS	
Operating Temperature (Options C or F)	T_{OP}	0° to 70° or -40 to +85°			°C	1,3

1. See Standard Frequencies and Ordering Information.
2. Parameters are tested with production test circuit below (Fig 2).
3. Parameters are tested at ambient temperature with test limits guard banded for specified operating temperature.
4. Measured from 20% to 80% of a full output swing (Fig 3).
5. Not tested in production, guaranteed by design, verified at qualification.
6. The FX-427 phase noise and jitter performance can be optimized for specific applications. Please consult with Vectron's Application Engineers for more information.
7. LVCMOS input signal levels are valid for input frequencies < 100 MHz.

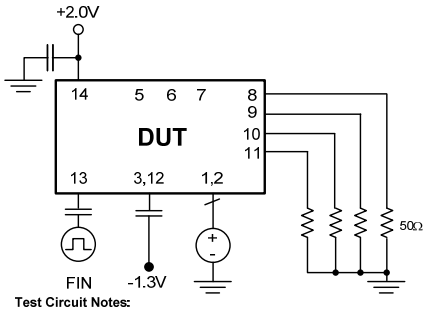


Figure 2. Test Circuit

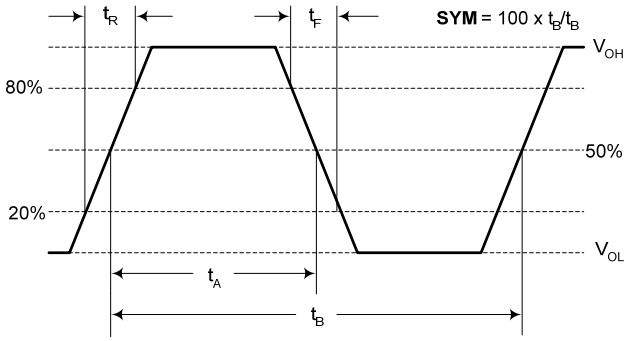


Figure 3. LVPECL Waveform

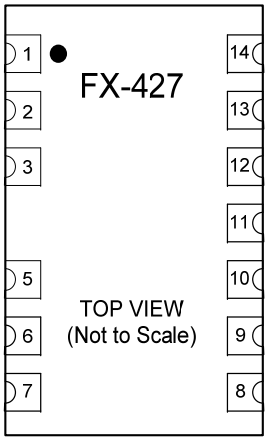


Figure 4. Pin Configuration

Table 2. Pin Out

Pin #	Symbol	I/O	Level	Function
1	SEL0	I	LVCMOS	Frequency Select - see table 3
2	SEL1	I	LVCOMS	Frequency Select – see table 3
3	GND	GND	Supply	Case and Electrical Ground
4				Not present
5	VMON	O	Analog (0 – Vcc)	VCXO Control Voltage Monitor Under locked conditions VMON should be > 0.3V and <3.0V. The input frequency may be out of range if the voltage exceeds these levels.
6	OD	I	LVCMOS	Output Disable Disabled = Logic “1” Enabled = Logic “0” or no connect
7	LD	O	LVCMOS	Lock Detect Locked = Logic “1” Loss of Lock = Logic “0”
8	FOUT1	O	LCPECL	Frequency Output – Primary
9	CFOUT1	O	LVPECL	Complimentary Frequency Output - Primary
10	FOUT2	O	LVPECL	Divided-Down VCSO/VCXO Output, or Disabled
11	CFOUT2	O	LVPECL	Complimentary Divided-Down VCSO/VCXO Output, or Disabled
12	GND	GND	Supply	Case and Electrical Ground
13	FIN	I	LVCMOS or LVPECL	Input Frequency – AC Coupled[1]
14	VCC	VCC	Supply	Power Supply Voltage (3.3 V ±5%)

[1] LVCMOS input signal levels are valid for input frequencies < 100 MHz.

Table 3. Control Logic (LVCMOS)

SEL0	SEL1	CLOCK INPUT
0	0	FIN_1
0	1	FIN_2
1	0	FIN_3
1	1	FIN_4

Outline Diagram

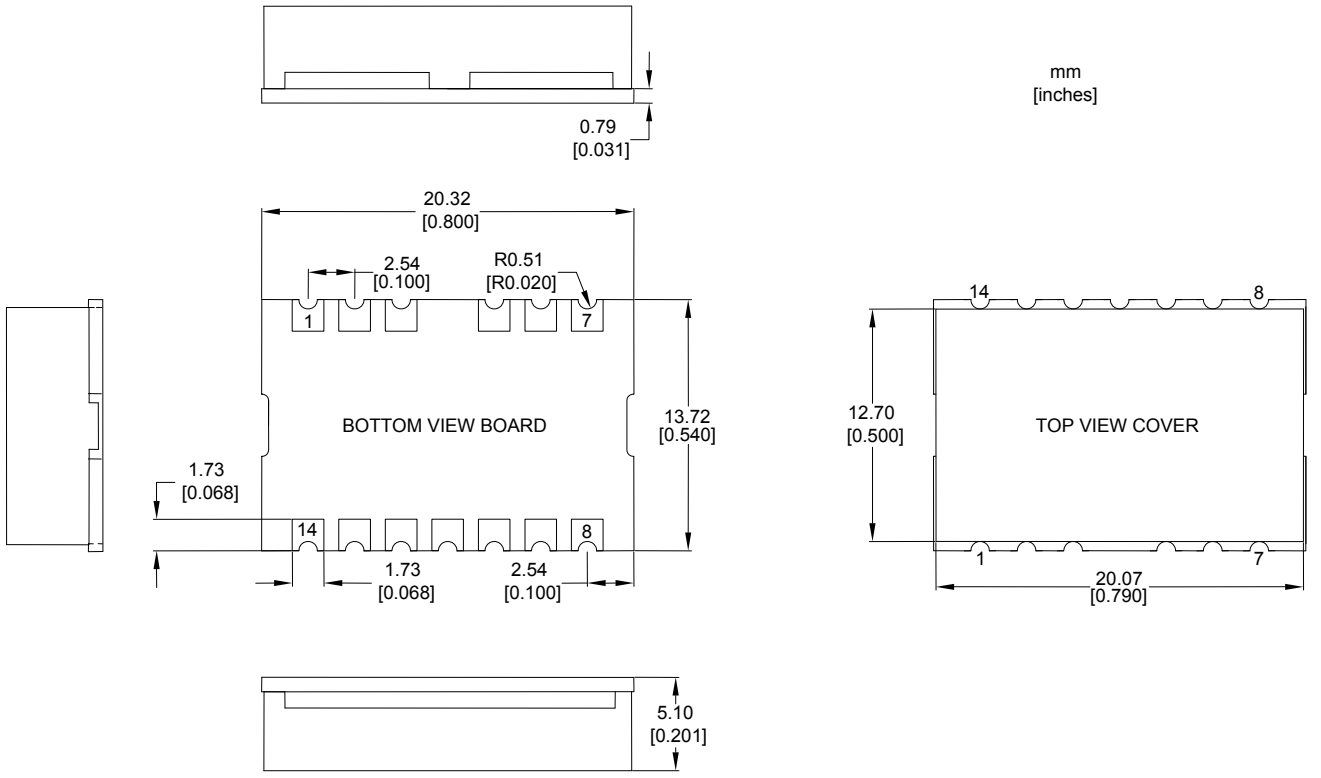


Figure 5.

Suggested Pad Layout

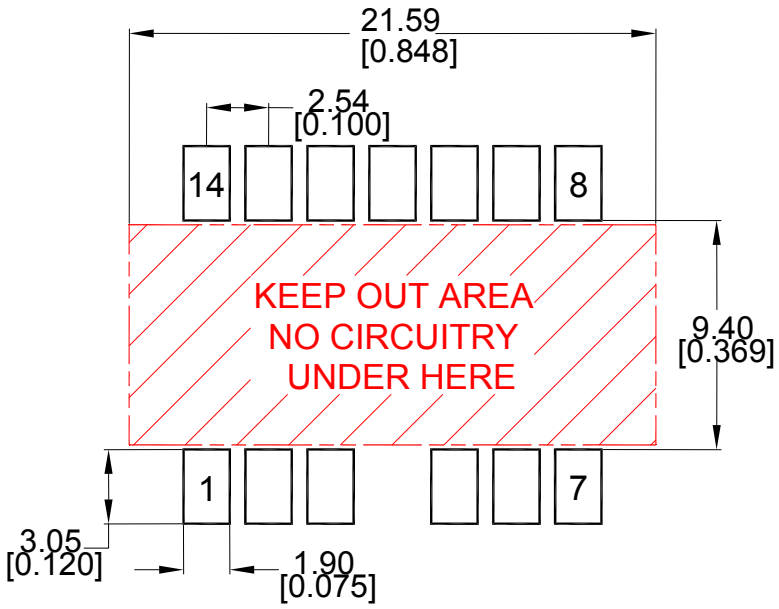


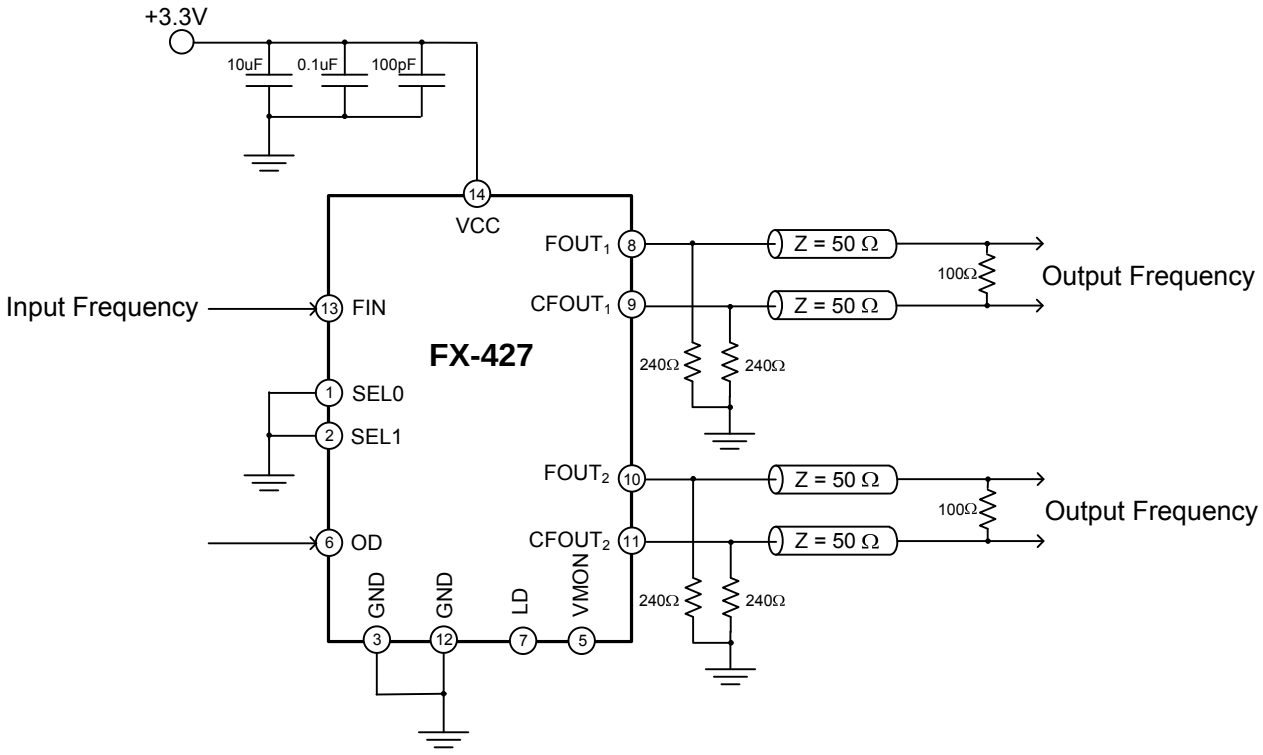
Figure 6.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T_{LS}	260/40	°C/sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Suggested Output Load Configurations



LV-PECL to LV-PECL: For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The FX-427 family is undergoing the following qualification tests:

Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Handling Precautions

Although ESD protection circuitry has been designed into the FX-427 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation

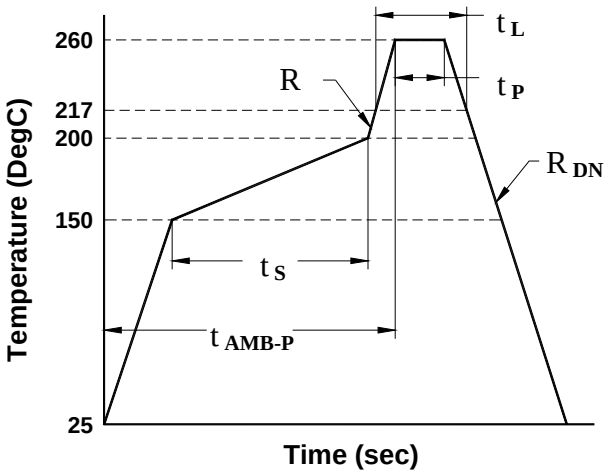
ESD Ratings

Model	Minimum	Conditions
Human Body Model	500 V	MIL-STD 883, Method 3015
Charged Device Model	500 V	JEDEC, JESD22-C101

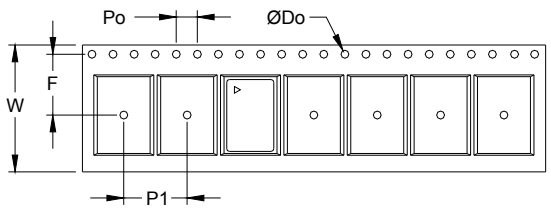
Reflow Profile (IPC/JEDEC J-STD-020C)

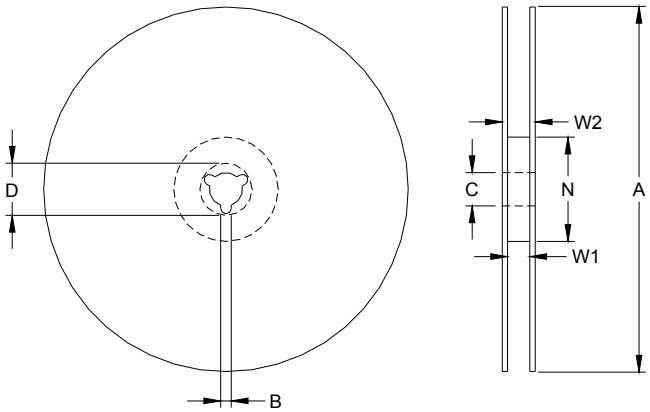
Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The FX-427 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-427 should not be subjected to a wash process that will immerse it in solvents. NO CLEAN is the recommended procedure. The FX-427 has been designed for pick and place reflow soldering. The FX-427 may be reflowed once and should not be reflowed in the inverted position.



Tape and Reel





Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	Reel
FX-427	32	14.2	1.5	4	20	330	1.5	13	20.2	100	44.4	50.4	200

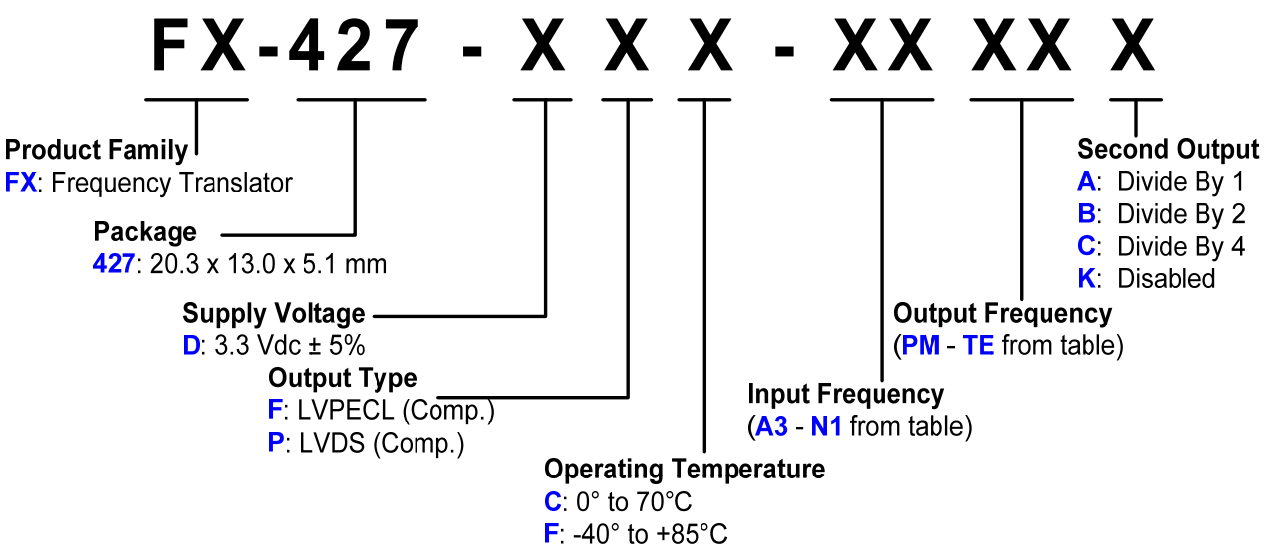
Vectron plans to offer both tape-n-reel and matrix trays as packaging options for the FX-427. The standard shipping container for volume production is a matrix tray. The trays are 100% recyclable and offer the added feature that they can be continuously fed into a pick-n-place machine.

Standard Frequencies (MHz)

0.0008	AN	3.2500	BC	19.6990	DK	41.6571	KP	80.0000	K9	334.6630	RB	805.6640	TA
0.0010	A1	3.3750	BH	19.7190	DH	41.8329	KT	80.5664	KJ	336.0810	RC	809.0630	TE
0.0020	AR	3.8400	B7	19.9219	ED	42.0000	JB	82.1777	KL	353.6760	RD	819.2000	TH
0.0032	AG	4.0000	BN	20.0000	E2	42.0102	KV	82.9440	K6	375.0000	RF	821.7770	TF
0.0040	A2	4.0960	B5	20.1416	E3	42.5000	JC	83.3143	KN	409.6000	RE		
0.0080	A3	5.0000	C6	20.4800	E4	42.6600	JZ	83.6658	KR	491.5200	PM		
0.0095	AU	5.1200	CD	20.5444	EF	44.2095	KX	84.0203	KU	531.0000	PH		
0.0100	A6	6.1440	CG	20.7135	E1	44.4343	LF	88.4191	KW	531.2500	P8		
0.0156	AL	6.2914	CC	20.8285	EG	44.6218	JW	97.5000	KE	568.9280	PJ		
0.0157	AD	6.2915	CF	20.8286	EB	44.7360	J3	100.0000	L8	569.1960	P9		
0.0158	AC	6.3120	C7	20.9165	EH	44.9280	JE	105.0000	L6	595.0560	PL		
0.0160	A4	6.4800	C2	21.0051	EJ	45.1584	JG	106.2500	L9	600.0000	PR		
0.0250	BR	6.7500	CB	22.0000	E9	45.8240	JM	108.0000	LA	622.0800	P2		
0.0400	AP	7.6800	C9	22.1048	EK	46.7200	JK	110.0000	L1	624.6930	PD		
0.0441	AA	7.7760	C5	22.2171	E5	46.8750	JY	112.0000	L2	624.7040	P6		
0.0480	AB	8.1920	C3	22.5792	E8	48.0000	JV	114.0000	L3	625.0000	P3		
0.0481	AV	9.2160	CH	24.0000	EC	49.1520	J7	120.0000	LC	627.3290	P7		
0.0500	BT	9.7200	C8	24.5760	E6	49.4080	J2	122.8800	LB	629.9870	PA		
0.0640	A5	9.7500	CE	24.7040	E7	50.0000	JD	124.4160	L7	637.5000	PG		
0.0800	A9	9.8304	C1	25.0000	F7	50.0480	KD	125.0000	L4	640.0000	PN		
0.1000	AH	10.0000	C4	25.1658	F8	51.8400	J4	130.0000	LD	644.5310	P4		
0.1280	AX	10.2300	DP	25.6000	F6	52.0000	JP	139.2640	L5	647.2390	PE		
0.2430	A8	10.2400	DM	25.9200	F2	53.3300	JU	150.0000	M8	647.2500	PK		
0.2560	AM	10.4143	DV	26.0000	F3	54.7460	JL	150.1440	M6	649.9700	PF		
0.3200	AW	10.4582	DU	27.0000	F4	55.0000	JX	155.5200	M2	657.4210	PB		
0.3840	AY	10.4872	DN	28.7040	F1	60.0000	JR	156.2500	M3	665.6250	PC		
0.4000	AF	10.9490	DG	29.4912	F5	61.3800	KY	159.3750	M7	666.5140	P5		
0.4800	AK	10.9500	DJ	29.5000	F9	61.4400	J5	160.0000	M1	669.1280	R2		
0.5000	BP	11.1840	DF	30.0000	HE	62.2080	J8	161.1320	M4	669.3260	R3		
0.5120	AJ	12.2880	D8	30.7200	H1	62.5000	J9	164.3550	M9	669.6420	R1		
0.6555	AE	12.3077	DY	30.8800	HF	62.9145	LE	166.6280	M5	670.8380	R7		
0.7720	AT	12.3520	D1	31.2500	H8	63.3600	JJ	167.3310	N2	672.1620	R5		
0.9600	A7	12.8000	D2	32.0000	H2	63.8976	JN	168.0400	N3	673.4560	RA		
1.0000	BB	13.0000	D3	32.7680	H3	64.0000	JT	170.0000	N4	684.2550	R9		
1.0240	B2	13.5000	DT	33.0000	H7	64.1520	JH	176.8380	NA	690.5690	R4		
1.2150	BU	14.8352	DL	33.3330	HC	65.5360	J6	182.0160	N8	693.4830	R6		
1.2288	BK	15.0000	D4	34.3680	H6	66.0000	JA	187.5000	N5	693.7500	R8		
1.2500	BG	15.0336	DR	34.5600	HB	70.0000	KB	195.0000	N7	704.3800	TG		
1.3333	BF	15.3600	DW	36.8640	HG	70.6560	KC	200.1920	N6	707.3520	TC		
1.5000	BE	16.0000	D9	37.0560	H4	71.6100	KF	201.4160	N1	710.9480	T2		
1.5440	B3	16.3840	D5	37.1250	H9	73.7280	K8	245.7600	N9	716.5730	T1		
1.9200	B1	17.1840	DE	37.5000	HK	74.1250	K1	262.1440	NB	718.7500	T5		
2.0000	B8	18.4320	D7	38.8800	H5	74.1758	KA	300.0000	PT	719.7340	T3		
2.0480	B4	18.5280	DC	39.0625	HH	74.2500	K7	311.0400	P1	748.0700	T6		
2.3040	BD	18.7500	EE	39.3216	HD	75.0000	KH	312.5000	PU	750.0000	T7		
2.4576	BJ	19.2000	DD	39.8438	HJ	76.8000	K4	318.7500	PV	777.6000	T4		
2.5000	BM	19.3927	DX	40.0000	JF	77.7600	K2	320.0000	PP	779.5680	T8		
2.5575	B9	19.4400	D6	40.2831	KK	78.1250	K3	322.2650	PW	780.8810	TD		
3.0880	B6	19.5313	DZ	40.9600	J1	78.6432	K5	328.7110	PX	781.2500	T9		
3.2400	BL	19.6608	DB	41.0889	KM	79.6875	KG	333.2570	PY	796.8750	TB		

Note 1: Other frequencies available upon request.
Note 2: Not all combinations are possible.
Note 3: For multiple input frequencies, replace the Input Frequency Code with “SS” and denote the input frequencies following the part number.

Ordering Information



EXAMPLE: **FX-427-DFF-A3P2C**
FX-427, 3.3V, LVPECL output, -40° to +85°C, F_{IN1} = 8 kHz, F_{OUT1} = 622.08 MHz, F_{OUT2} = 155.52 MHz.

EXAMPLE: **FX-427-DFC-SSP2B, S = 2.048 MHz, 19.44 MHz, 77.76 MHz**
FX-427, 3.3V, LVPECL output, 0° to 70°C, F_{IN1} = 2.048 MHz, F_{IN2} = 19.44 MHz, F_{IN3} = 77.76 MHz, F_{OUT1} = 622.08 MHz, F_{OUT2} = 311.04 MHz

For Additional Information, Please Contact:

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Revision History:

Revision	Date	PLM Approval	Eng req'd	Engineer Approval	Date	Description
A	11/8/06	BW				Original Release
B	7/31/07	BW				Added clarification to input signal amplitude specification for LVCMOS. Frequency < 100 MHz.
C	8/22/07	BW				Updated test circuit. Updated frequency code listing. Added application circuit.