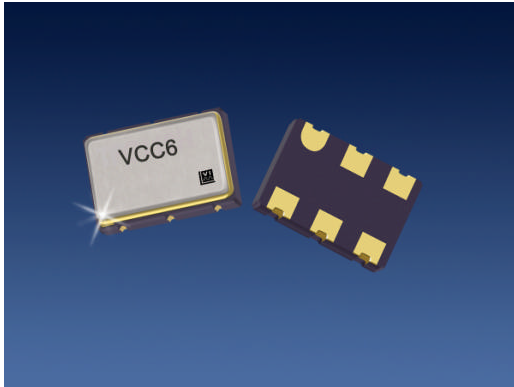



## VCC6-D

### 106M250/212M500 Dual Rate PECL and LVDS Oscillator



The VCC6-D Crystal Oscillator

#### Features

- 3.3V LVPECL or 3.3V LVDS
- Output frequency select
- Enable/Disable output for test and board debug
- Hermetically sealed ceramic SMD package
- Excellent Power Supply Noise Rejection
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

#### Applications

- 1Gbps, 2Gbps, 4 Gbps Fiber Channel
- Storage Area Network
- Host Bus Adapter
- RAID controller

#### Description

Vectron's VCC6-D Crystal Oscillator (XO) is quartz stabilized square wave generator with a LV-PECL or LVDS output, operating off a 3.3 volt supply.

The VCC6 uses high quality on-chip multiplier to multiply a 26.5625 crystal to either 106M250 or 212M500.

# VCC6-D, Dual Rate 106.250/212.500 LVPECL or LVDS XO

## Performance Characteristics

| Table 1. Electrical Performance  |                      |                   |          |                |          |
|--|----------------------|-------------------|----------|----------------|----------|
| Parameter  | Symbol               | Min               | Typical  | Max            | Units    |
| Frequency  | $f_O$                | 106.250 / 212.500 |          |                | MHz      |
| Supply Voltage <sup>1</sup>  | $V_{DD}$             | 3.0               |          | 3.6            | V        |
| Supply Current, PECL<br>LVDS   | $I_{DD}$             |                   | 50<br>53 | 65<br>67       | mA       |
| Output Logic Levels, 0/70°C<br>PECL Output Logic High <sup>2</sup><br>PECL Output Logic Low <sup>2</sup> | $V_{OH}$<br>$V_{OL}$ | $V_{DD}-1.025$    |          | $V_{DD}-1.620$ | V<br>V   |
| LVDS Output High Voltage   | $V_{OH}$             |                   |          | 1.475          | V        |
| LVDS Output Low Voltage  | $V_{OL}$             | 0.925             |          |                | V        |
| LVDS Differential Output Voltage   | $ V_{OD} $           | 250               |          | 400            | mV       |
| LVDS Change in Magnitude   | $\Delta V_{OD} $     |                   |          | 25             | mV       |
| LVDS Offset Output Voltage   | $V_{OS}$             | 1.125             |          | 1.275          | V        |
| LVDS Change in Magnitude of Output Offset  | $\Delta V_{OS} $     |                   |          | 25             | mV       |
| Transition Times<br>Rise Time <sup>2</sup><br>Fall Time <sup>2</sup>                                     | $t_R$<br>$t_F$       |                   |          | 600<br>600     | ps<br>ps |
| Symmetry or Duty Cycle <sup>3</sup>  | SYM                  | 45                | 50       | 55             | %        |
| Operating temperature  |                      | -10/70            |          |                | °C       |
| Stability ( <i>ordering option</i> ) <sup>4</sup>  |                      | +/-50 or +/-100   |          |                | ppm      |
| RMS Jitter, 12kHz to 20 MHz, $f_O < 200\text{MHz}$   |                      |                   | 0.75     |                | pS       |
| Cycle-Cycle Jitter, rms  |                      |                   | 4        |                | pS       |
| Output Enabled <sup>5</sup> , Frequency Select   | $V_{IH}$             | 2                 |          |                | V        |
| Output Disabled <sup>5</sup> , Frequency Select  | $V_{IL}$             |                   |          | 0.8            | V        |
| Logic Input Current, High  | $I_{IH}$             | -10               |          | +10            | uA       |
| Logic Input Current, Low   | $I_{IL}$             | -50               |          | +50            | uA       |
| Package Size   |                      | 5.0 x 7.5 x 1.8   |          |                | mm       |

1. A 0.01 uF and a 0.1 uF capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 1 defines these parameters. Figure 2 illustrates the operating conditions under which these parameters are tested and specified.
3. Symmetry is measured defined as  $V_s$ , On Time/Period.
4. Includes calibration tolerance, operating temperature, supply voltage variations, aging (40 degreesC/10 years) and shock and vibration (not under operation). Aging budget is +/-5 ppm.
5. Output will be enabled if enable/disable is left open. Output frequency=106M250 if FREQ is left open.

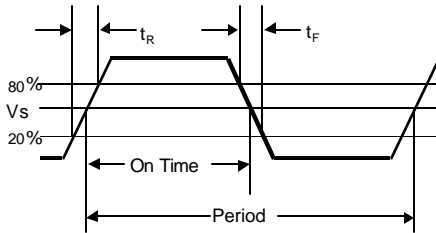
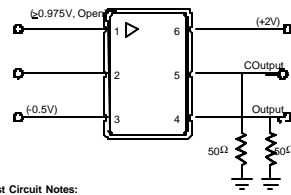


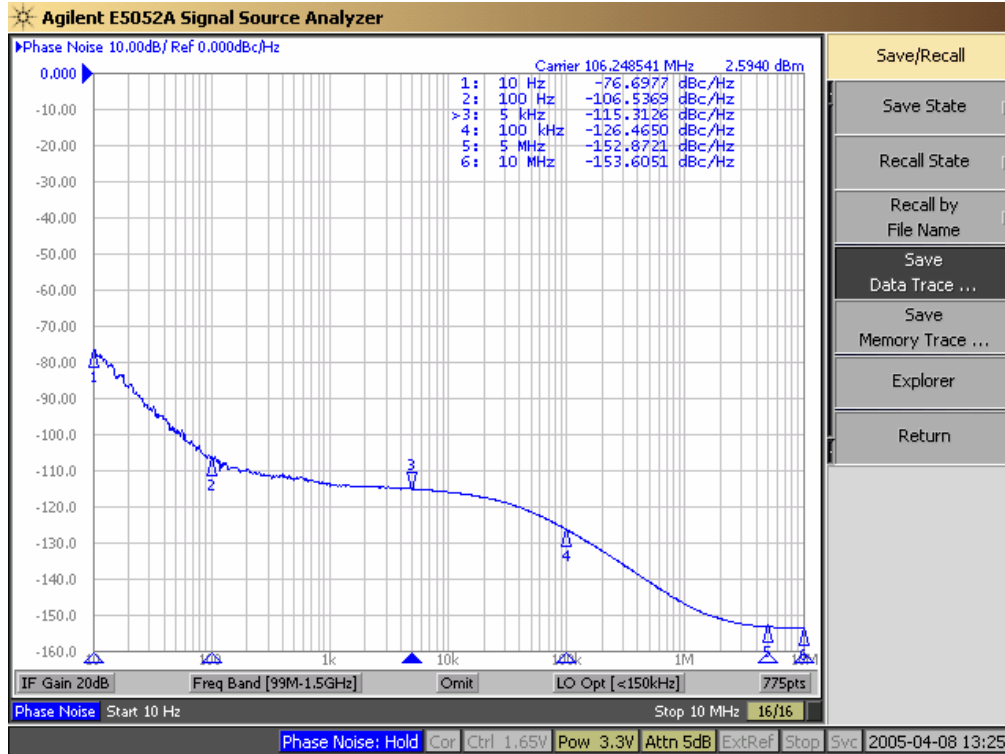
Figure 1. Output Waveform



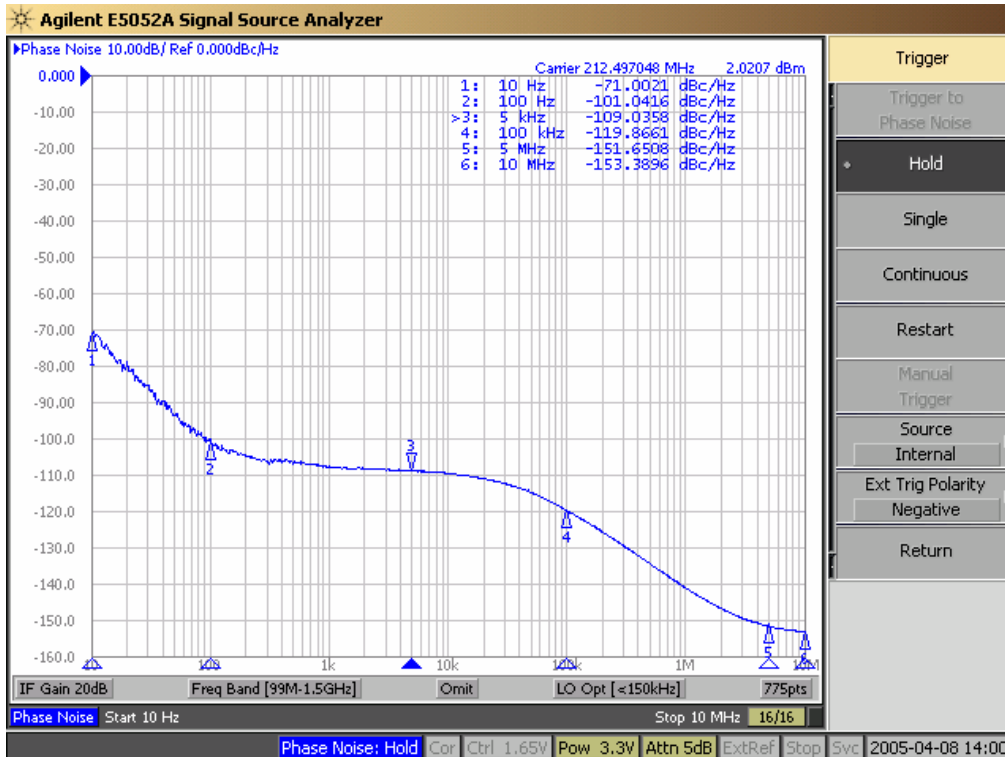
Test Circuit Notes:  
 1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 0.5V.  
 2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.  
 3) 50Ω Terminations are Within Test Equipment.

Figure 2. Typical Output Test Conditions (25±5°C)

# VCC6-D, Dual Rate 106.250/212.500 LVPECL or LVDS XO



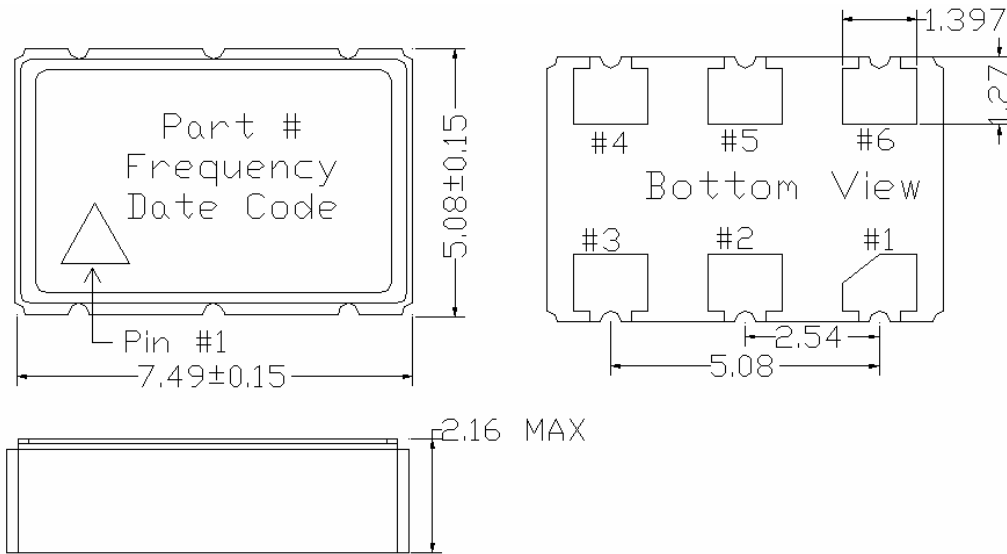
Typical Phase Noise at 106.25MHz



Typical Phase Noise at 212.5MHz

# VCC6-D, Dual Rate 106.250/212.500 LVPECL or LVDS XO

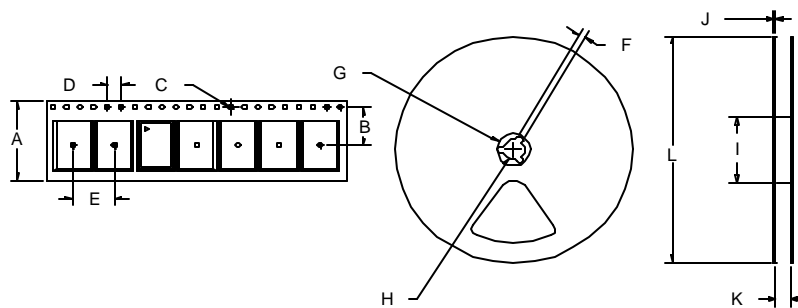
## Outline Diagram and Pin Out



Contact pads are gold over nickel

| Pin # | Symbol   | Function  |
|-------|----------|---|
| 1     | E/D      | Output disabled when = logic 0, Output Enabled when = logic 1<br>Device has an internal pull-up resistor. |
| 2     | FREQ     | Output = 106M25 when = logic 1, 212M50 when = logic 0<br>Device has as an internal pull-up resistor.      |
| 3     | GND      | Ground  |
| 4     | $f_o$    | Output Frequency  |
| 5     | $Cf_o$   | Complementary Output Frequency  |
| 6     | $V_{DD}$ | Supply Voltage  |

## Tape and Reel



| Tape and Reel Dimensions (mm) |    |     |     |   |                 |      |      |    |    |   |      |     |            |
|-------------------------------|----|-----|-----|---|-----------------|------|------|----|----|---|------|-----|------------|
| Tape Dimensions               |    |     |     |   | Reel Dimensions |      |      |    |    |   |      |     | # Per Reel |
| Product                       | A  | B   | C   | D | E               | F    | G    | H  | I  | J | K    | L   |            |
| VCC6                          | 12 | 5.5 | 1.5 | 4 | 8               | 1.78 | 20.6 | 13 | 55 | 6 | 12.4 | 178 | 250        |

## VCC6-D, Dual Rate 106.250/212.500 LVPECL or LVDS XO

### Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

| Parameter           | Symbol               | Ratings                      | Unit |
|---------------------|----------------------|------------------------------|------|
| Power Supply        | V <sub>DD</sub>      | -0.5 to +5.0                 | Vdc  |
| Enable/Disable      | V <sub>IN</sub>      | -0.5 to V <sub>DD</sub> +0.5 | Vdc  |
| Storage Temperature | T <sub>storage</sub> | -55/125                      | °C   |

### Reliability

The VCC6 qualification tests will include the following:

| Parameter              | Conditions              |
|------------------------|-------------------------|
| Mechanical Shock       | MIL-STD-883 Method 2002 |
| Mechanical Vibration   | MIL-STD-883 Method 2007 |
| Solderability          | MIL-STD-883 Method 2003 |
| Gross and Fine Leak    | MIL-STD-883 Method 1014 |
| Resistance to Solvents | MIL-STD-883 Method 2016 |

### Handling Precautions

Although ESD protection circuitry has been designed into the the VCC6, proper precautions should be taken when handling and mounting. VI employs a Human Body Model and a Charged-Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance = 1.5kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes.

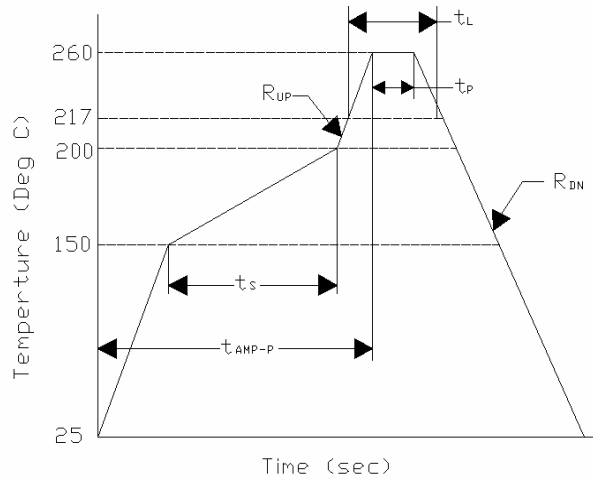
| Model                | Minimum | Conditions              |
|----------------------|---------|-------------------------|
| Human Body Model     | 1000    | MIL-STD-883 Method 3115 |
| Charged Device Model | 1000    | JESD 22-C101            |

# VCC6-D, Dual Rate 106.250/212.500 LVPECL or LVDS XO

## Suggested IR profile

The VCC6 has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements and parameters are listed in Table 7. The VCC6 is hermetically sealed so an aqueous wash is not an issue.

| Parameter                | Symbol      | Value                   |
|--------------------------|-------------|-------------------------|
| PreHeat Time             | $t_s$       | 60 sec Min, 180 sec Max |
| Ramp Up                  | $R_{UP}$    | 3 °C/sec Max            |
| Time Above 217 °C        | $t_L$       | 60 sec Min, 150 sec Max |
| Time To Peak Temperature | $t_{AMB-P}$ | 480 sec Max             |
| Time At 260 °C (max)     | $t_P$       | 10 sec Max              |
| Time At 240 °C (max)     | $t_{p2}$    | 60 sec Max              |
| Ramp Down                | $R_{DN}$    | 6 °C/sec Max            |



# VCC6-D, Dual Rate 106.250/212.500 LVPECL or LVDS XO

| Frequencies (MHz) which are being developed |  |  |  |  |
|---|--|--|--|--|
| 106.25/212.50                               |  |  |  |  |
|   |  |  |  |  |
|   |  |  |  |  |
|   |  |  |  |  |

Other frequencies may be available upon request. Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

## Ordering Information

### VCC6-Dxx – 106M25

**Product Family**

Crystal Oscillator

**Supply Voltage, Output**

D= Dual Rate

**PECL/LVDS**

Q: 3.3volt, LVPECL

L: 3.3volt, LVDS

**Frequency MHz**

example: 106M250= 106.25/212.50MHz

**Stability Options/Temperature**

A: +/-100ppm/ -10 to 70 C

B: +/-50ppm/-10 to 70 C

Also available is a VCC6-1091 which is fixed at 212.500MHz, LVPECL, 50ppm over -10 to 70C, and a VCC6-1121 which is fixed at 212.500MHz, LVPECL and is 100ppm over -10 to 70C.

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VCC6-D (REVISION DATE: April 18 2005)